

IN THE CLAIMS:

Kindly replace the claims of record with the following full set of claims:

1. (Currently amended) A device applicable for non-volatile memory purpose or latch-up circuits, the device comprising:

[[-]] a selection device having a control electrode and a first dielectric layer place thereon insulating the control electrode from the rest of the selection device, and

[[-]] a storage device comprising a first electrode and a second dielectric layer deposited on the first electrode, wherein the first dielectric layer of the selection device and the second dielectric layer of the storage device are individual parts of a one and the same ferroelectric layer wherein the control electrode and the first electrode of the storage device are electrically isolated elements of a same conductive layer.

2. (Currently amended) A device according to claim 1, wherein the selection device is a transistor comprising a gate electrode, a gate dielectric and a drain and a source, wherein the gate electrode is representative of the control electrode and the gate dielectric is representative of the first dielectric layer, the source and drain being positioned on the gate dielectric and containing a channel therebetween, and wherein the storage device is a capacitor further comprising a first electrode, a dielectric layer and a second electrode, deposited on the second dielectric layer, wherein the gate dielectric of the transistor and the dielectric layer of the capacitor are individual parts of one and the same ferroelectric layer.

3. (Currently amended) The device according to claim [[1]] 2, wherein the gate electrode of the transistor and the first electrode of the capacitor are individual parts of a first conductive layer.

4. (Currently amended) The device according to claim [[1]] 2, wherein the drain and source of the transistor and the second electrode of the capacitor are individual parts of a second conductive layer.

5. (Currently amended) The device according to claim [[1]] 2, wherein one of the first and second electrode of the capacitor is electrically connected to one of the drain, the source [[or]] and the gate of the transistor.

6. (Currently amended) The device according to claim [[1]] 2, wherein the gate electrode, the drain and the source of the transistor and the first electrode and the second electrode of the capacitor are formed of PEDOT/PSS.

7. (Previously presented) The device according to claim 1, the device furthermore comprising a semiconductive layer.

8. (Previously presented) The device according to claim 7, wherein the semiconductive layer is an organic semiconductive layer.

9. (Previously presented) The device according to claim 1, wherein the ferroelectric layer comprises a hole.

10. (Withdrawn) A method for processing device applicable for non-volatile memory purposes or latch-up circuits comprising a selection device comprising a control electrode, a first dielectric layer and a first and second main electrode, and a storage device comprising a first electrode, a second dielectric layer and a second electrode, the method comprising:

- providing and patterning of a first conductive layer onto a substrate, thus forming the first electrode of the storage device and the control electrode of the selection device,
- providing and patterning of a ferroelectric layer on the patterned first conductive layer, thus forming the first dielectric layer of the selection device and the second dielectric layer of the storage device, and

- providing and patterning of a second conductive layer on the patterned ferroelectric layer, thus forming the second electrode of the capacitor and the first and second main electrode of the selection device.

11. (Withdrawn) The method according to claim 10, wherein providing of the ferroelectric layer is providing of a ferroelectric polymer layer.

12. (Withdrawn) The method according to claim 10, wherein patterning the ferroelectric layer comprises crosslinking the ferroelectric layer.

13. (Currently amended) A processing producing the device (30) produced by the method of claim [[10]] 1 and applicable for non-volatile memory purposes or latch-up circuits, the device comprising:

a selection device (22) having a control electrode (13) and a first dielectric layer insulating the control electrode from the rest of the selection device, and

a storage device (23) comprising a first electrode and a second dielectric layer deposited thereon, wherein the first dielectric layer of the selection device (22) and the second dielectric layer of the storage device (23) are individual parts of a one and the same ferroelectric layer (14) wherein the control electrode and the first electrode of the storage device are electrically isolated elements of a same conductive layer.

14. (Withdrawn-currently amended) A process producing the device (30) of claim [[1]] 10, the process comprising the acts of:

[[-]] providing and patterning of a first conductive layer onto a substrate (10), thus forming the a first electrode (12) of the a storage device (23) and the a control electrode (13) of the a selection device (22),
[[-]] providing and patterning of a ferroelectric layer (14) on the patterned first conductive layer, thus forming the a first dielectric layer of the selection device (22) and the second dielectric layer of the storage device

(23), and

[--]] providing and patterning of a second conductive layer on the patterned ferroelectric layer (14), thus forming the second electrode (18) of the storage device capacitor (23) and the first (19) and a second (20) main electrode of the selection device (22).

15. (Withdrawn) The method of claim 10 wherein the method produces a processing device (30) applicable for non-volatile memory purposes or latch-up circuits, and comprising a selection device (22) comprising a control electrode (13), a first dielectric layer and a first (19) and second (20) main electrode, and a storage device (23) comprising a first electrode (12), a second dielectric layer and a second electrode (18).